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Analysis and Design of a Specialized Pipeline for Numerical Algorithms Implementation

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Abstract. **The numerical algorithms often bring a lot of elementary calculations which involve the fixed-point multiply, add and subtract operations. Many of these numerical and signal processing algorithms require repetitive use of multiply and accumulate operation. The contribution of the paper is to present the analysis and design of an FPGA-based specialized pipeline, in order to develop flexible (co)processors for applications in the field of numerical analysis and digital signal processing. Essentially, the paper focuses on some details of the analysis and design of the proposed pipeline structure. In particular, provided analysis considers the bus traffic utilization in the system. The obtained results are plotted for some specific parameters. The simulation results are also drawn. For this reason, the Altera Quartus software was used.**

Index Terms **— DSP, FPGA, multiply and accumulate operation, numerical algorithm, pipelining.**

I. INTRODUCTION

In scientific computation and signal processing (DSP), high-performance is strictly important. Essentially, these computations can be classified into compute-bound and input/output-bound computations. In a compute-bound calculation the number of arithmetic operations is much larger that the number of input and output elements (e.g. matrix multiplication). The computational tasks involved by algorithms in numerical analysis and DSP are typical of the compute-bound class. In addition, many algorithms in numerical computing and digital signal processing have a high regularity [1, 2, 6]. Hence, numerical methods with these characteristics are quite suitable for a specialized treatment.

To address the performance barrier of scientific computation and DSP, a standard approach in the past has been to increase the operating frequency of the processor. Other well known approaches to improve the performance include the use of additional processors, the use of specialized programmable processors or through the use of FPGA-based processor architectures. Adding additional devices to a system can be costly, especially under the requirements for system reliability.

On the other hand, modern FPGA circuits, with their ability to integrate multiple (co)processors in a single device, can provide advanced solutions to accelerate the performance. Another key advantage of modern FPGAs is the ability to adapt and quickly respond to changing application requirements. As a direct result of the above capabilities, FPGAs can be used to develop highly performance architectures for numerical analysis and DSP applications.

A new category of very high-performance programmable logic devices has been developed to address the un-met needs of system designers. The MathStar Field Programmable Object Array (FPOA) is an example of this category, offering many very useful capabilities [7]. Because of its high-performance, the FPOA is useful in a wide range of applications, including those in the areas of machine vision, medical imaging and image processing. These applications are built around extremely fast specialized building blocks.

The goal of this paper is to present the analysis and design of an FPGA-based specialized pipeline, in order to develop flexible (co)processors for numerical applications. First of all, background section focuses on the features and basics in the field. Then, basic sections are presented. At first, here we discuss some details of the analysis and design of the pipeline. Mainly, our analysis considers the bus traffic utilization in the system. Finally, we present simulation results and conclude the work in the last section.

II. BACKGROUND

The numerical algorithms often bring a lot of elementary calculations. Most of these elementary calculations involve the fixed-point multiply, add and subtract operations. Essentially, the differences between conventional and special-purpose processors involve optimization for specific arithmetic operations and data handling. Such processors are optimized to efficiently execute optimized operations which allow the efficient implementation of numerical processing algorithms. The input signals can be audio, image-based or simply numerical.

Many of these specialized numerical and DSP algorithms require repetitive use of the following operation group:

$$A = B \times C + D \qquad (1)$$

This operation group is clearly a multiply and an addition also known as a multiply and accumulate (MAC). This operation is so common that DSP processors have been optimized to implement one or more MAC operations during each processor instruction cycle. Data handling has also been given significant design attention. Extra buses have been added to processors to allow them to more efficiently handle internal and external data transfers. Pipelines and additional data paths and registers have also been added to speed up arithmetic operations and data transfers [3, 4].

Fore example, the fast Fourier transform (FFT) is one